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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,132	01/24/2000	William C. Moyer	SC10927TS	6776

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Harry A Wolin
Motorola INc Austin Intellectual Property
7700 West Parmer lane
MD TX32/PL02
Austin, TX 78729

EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 10/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/490,132	Applicant(s) MOYER, WILLIAM C.	
	Examiner Kim T. Huynh	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *September 3, 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

RUPAL DHARIA
PRIMARY EXAMINER

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-16 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-16 have been considered but are deemed to be moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6 and 9-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Arndt et al. (U. S Patent 5,701,495)

Arndt discloses:

a. As per claims 1,9 and 14,

- providing a first storage device having a plurality of inputs, each of the plurality of inputs being coupled by a respective physical conductor to one of a plurality of hardware-generated interrupt sources which selectively generate hardware interrupts and selectively storing the hardware interrupts, the first storage device

providing one or more hardware-generated interrupt signals. (col.18, lines 28-32)

- providing a second storage device having one or more inputs, each of the one or more inputs receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage device providing one or more software-generated interrupt signals (col.8, lines 56-67), (col.9, lines 1-13), (col.18, lines 20-27), (col.2, lines 26-43), (col.4, lines 27-32), (see abstract, lines 3-13)
- coupling logic circuitry to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an interrupt request signal which will cause an interrupt to occur in the data processing system (col.4, lines 25-35), (col.9, lines 14-17)
- a plurality of hardware interrupt sources; (col.18, lines 28-32)
- executing software with the data processing system to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources but with a priority which differs from the predetermined one of the

hardware-generated interrupt sources, thereby dynamically changing prioritization of servicing of interrupts in the data processing system; (col.9, lines 15-67), (col.10, lines 1-67), (col.11, lines 1-14)

b. As per claims 2 and 10, assigning an interrupt prioritization level to specific storage locations of the first storage device and the second storage device, the interrupt prioritization level of the plurality of hardware-generated interrupt source coupled to the first storage device being permanently assigned, but assignment of the interrupt prioritization level of interrupt sources associated with the second storage device being variable by software control. (col.4, lines 27-32), (col.4, lines 53-61), (col.2, lines 26-43).

c. As per claim 3, assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupt and having a corresponding interrupt prioritization level (col.3, lines 36-68), (col.4, lines 1-67).

d. As per claim 4, assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from same interrupt sources generating hardware interrupts and having an interrupt prioritization level which differs from the interrupt prioritization level of the plurality of hardware-generated interrupt sources coupled to the first storage device (col.4, lines 17-32)

e. As per claim 6, changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt. (col.12, lines 56-65), (col.9, lines 52-67), (col.10, lines 1-9)

f. As per claim 11, a software-generated interrupt signal of higher priority than a currently executing hardware-generated interrupt signal is provided to the logic circuitry prior to completion of an associated hardware interrupt servicing, and the data processing system suspends processing of the hardware interrupt servicing to process an associated software interrupt servicing. (col.9, lines 15-67), (col.10, lines 1-53), (col.12, lines 10-31)

g. As per claims 12 and 16, a mask register coupled to the hardware interrupt storage device and the software interrupt storage device for selectively preventing hardware-generated interrupt signals and software-generated interrupt signals from propagating to the logic circuitry. (col.12, lines 10-31)

h. As per claim 13, the hardware interrupt storage device and the software interrupt storage device are each implemented as latch circuits. (col.4, lines 53-61)

i. As per claim 15, generating the predetermined software-generated interrupt signal which emulates the predetermined one of the hardware-generated interrupt sources while another hardware-generated interrupt is being serviced,

the predetermined software-generated interrupt signal having a priority which is higher than the other hardware-generated interrupt being serviced; (col.9, lines 15-67), (col.10, lines 1-67), (col.11, lines 1-13)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5,7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al. (U.S Patent 5,701,495) in view of Koscal et al. (U.S Patent 6,412,081)

Arnedt discloses all the limitations as above except the limitation that the changing interrupt servicing from hardware-generated to software-generated interrupt, combination circuitry to determining whether to pass the hardware-generated and software-generated interrupts and determining priority between two interrupts as claimed as claims 5,7 and 8.

However, Koscal discloses a predetermined bit of the PSR is placed in a defined state responsive to the occurrence of a condition. (see abstract, lines 8-25), Furthermore, the output of the compare circuit changes state whenever the data matches value, depending on the specific implementation. (col.7, lines 49-63). The particular state of the bit is determined the responsive to whether an interrupt is a hardware or software interrupt. (col.9, lines 52-67), (col.10, lines 1-13)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Koscal's teaching into Arndt's method to include the changing interrupt servicing from hardware-generated to software-generated interrupt, combination circuitry to determining whether to pass the hardware-generated and software-generated interrupts and determining priority between two interrupts as to be a greater flexibility and compatible with the latest advancements in the computer system technology.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sleeman et al. [USPN 6,397,284] discloses apparatus and method for handling peripheral device interrupts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703)305-3477 or via e-mail addressed to [Peter.Wong@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Oct. 25, 2002

RUPAL DHARIA
PRIMARY EXAMINER